WHAT IS CLAIMED IS:

1. An MPEG data recording apparatus comprising:

an IEEE 1394 interface having an input terminal connected to an external device and serving to receive MPEG data output from said external device and a recording control code output from said external device with delay after receiving said MPEG data and to output at least said MPEG data and said recording control code from an output terminal;

an MPEG data detecting section having an input terminal connected to said output terminal of said IEEE 1394 interface and serving to detect that said MPEG data are present validly or not and to output a data detection signal from an output terminal thereof when said MPEG data are present validly;

an FIFO buffer section having an input terminal connected to said output terminal of said IEEE 1394 interface and a control terminal and serving to temporarily store said MPEG data;

a data recording section having an input terminal connected to an output terminal of said FIFO buffer section and a control terminal and serving to record said MPEG data output from said FIFO buffer section; and

a buffer control section having an input terminal connected to said output terminal of said IEEE 1394 interface and said output terminal of said MPEG data detecting section, and serving to output a signal for giving a command for starting an FIFO operation to said control terminal of said FIFO buffer section and to output a signal for giving a command for stopping a recording operation to said control terminal of said data recording section in response to receipt of said data detection signal, and to output a signal for giving a command for reading said MPEG data to said control terminal of said FIFO buffer section and to output a signal for giving a command for starting said

recording operation to said control terminal of said data recording section in response to receipt of said recording control code.

2. The MPEG data recording apparatus according to claim 1, wherein

said IEEE 1394 interface also receives and outputs a recording stop control code output from said external device with delay after receiving said recording control code, and

said buffer control section outputs:

(i) a signal to said control terminal of said FIFO buffer section, in response to said receipt of said recording stop control code, for giving a command for stopping said FIFO operation after outputting all said MPEG data which have been stored in said FIFO buffer section when receiving said recording stop control code to said input terminal of said data recording section; and

(ii) a signal to said control terminal of said data recording section, in response to said receipt of said recording stop control code, for giving a command for stopping said recording operation after recording all said MPEG data which have been stored in said FIFO buffer section when receiving said recording stop control code.

3. The MPEG data recording apparatus according to claim 2, wherein

said IEEE 1394 interface generates a clock to be a reference of said MPEG data and outputs said clock together with said MPEG data from said output terminal, and

said MPEG data detecting section receives said MPEG data and said clock and detects said MPEG data synchronously with said clock, thereby detecting that a specific data pattern appears every constant cycle or not and outputting said data detection signal when said specific data pattern appears.

4. The MPEG data recording apparatus according to claim 2, wherein

said IEEE 1394 interface generates an MPEG data valid signal indicating that a received signal is said MPEG data and outputs said MPEG data valid signal together with said MPEG data from said output terminal, and

said MPEG data detecting section detects that said MPEG data are present validly or not based on said MPEG data valid signal thus received.

5. The MPEG data recording apparatus according to claim 2, wherein

said MPEG data detecting section detects presence of a signal synchronous with said MPEG data and a state in which said synchronizing signal appears every constant cycle, thereby deciding that said MPEG data are present validly to output said data detection signal.

6. The MPEG data recording apparatus according to claim 2, further comprising:

a data rate detecting section having an input terminal connected to said output terminal of said IEEE 1394 interface and serving to detect a data volume to be input per unit time as data rate information from said MPEG data,

wherein said input terminal of said buffer control section is also connected to an output terminal of said data rate detecting section,

said buffer control section has a delay time for which a user operates a control panel on said external device to issue a command for a recording start operation and said buffer control section then receives said recording control code, and

said buffer control section multiplies said delay time by said data rate information to calculate a data volume to be stored and updated in said FIFO buffer

section and determines addresses of a read pointer and a write pointer of said FIFO buffer section based on said data volume thus calculated, thereby setting said determined addresses to said FIFO buffer section in response to receipt of said data detection signal and said data rate information.

7. An MPEG data recording apparatus comprising:

an IEEE 1394 interface having an input terminal connected to an external device and serving to receive MPEG data output from said external device and a recording control code output from said external device with delay after receiving said MPEG data and to output at least said MPEG data and said recording control code from an output terminal;

MPEG data detecting means, having an input terminal connected to said output terminal of said IEEE 1394 interface, for detecting that said MPEG data are present validly or not and for outputting a data detection signal from an output terminal thereof when said MPEG data are present validly;

FIFO buffer means, having an input terminal connected to said output terminal of said IEEE 1394 interface and a control terminal, for temporarily storing said MPEG data;

data recording means, having an input terminal connected to an output terminal of said FIFO buffer means and a control terminal, for recording said MPEG data output from said FIFO buffer means; and

buffer control means, having an input terminal connected to said output terminal of said IEEE 1394 interface and said output terminal of said MPEG data detecting means, for outputting a signal for giving a command for starting an FIFO operation to said control terminal of said FIFO buffer means and outputting a signal for

giving a command for stopping a recording operation to said control terminal of said data recording means in response to receipt of said data detection signal, and for outputting a signal for giving a command for reading said MPEG data to said control terminal of said FIFO buffer means and outputting a signal for giving a command for starting said recording operation to said control terminal of said data recording means in response to receipt of said recording control code.

8. The MPEG data recording apparatus according to claim 7, wherein

said IEEE 1394 interface also receives and outputs a recording stop control code output from said external device with delay after receiving said recording control code, and

said buffer control means outputs:

(i) a signal to said control terminal of said FIFO buffer means, in response to said receipt of said recording stop control code, for giving a command for stopping said FIFO operation after outputting all said MPEG data which have been stored in said FIFO buffer means when receiving said recording stop control code to said input terminal of said data recording means; and

(ii) a signal to said control terminal of said data recording means, in response to said receipt of said recording stop control code, for giving a command for stopping said recording operation after recording all said MPEG data which have been stored in said FIFO buffer means when receiving said recording stop control code.